a third circuit coupled to the second circuit to detect one of a physical characteristic, temperature and voltage of the device.

4. (Original) The device of claim 3, wherein the third circuit encodes a set of detected conditions.

5. (Original) The device of claim 1, wherein the first circuit comprises an on die resistor.

6. (Original) The device of claim 5, wherein the on die resistor is a polyresistor.

7. (Original) A device comprising:

a set of transistors on die;

a first set of polyresistors coupled to the set of transistors;

a second set of polyresistors coupled to the first set of polyresistors, the first and second set of polyresistors having a predefined total resistance and predefine on die area; and

an input pad coupled to the second set of polyresistors..

8. (Original) The device of claim 7, wherein if the first set of polyresistors has a higher resistance than the second set of polyresistors then the device has a wider range of programmable resistances than if the first and second set of polyresistors had equal resistance.

9. (Original) The device of claim 7, wherein if the second set of polyresistors has a higher resistance than the first set of polyresistors then the device has a greater linearity of resistance during transition of a signal from a first voltage to a second voltage that is received at the input pad than if the first and send set of resistors had equal resistance.

10. (Original) An apparatus comprising:

a test block to determine a condition on a chip;

an encoder to encode the condition; and

a compensation circuit to adjust an on die termination circuit based on a first encoded condition.

11. (Original) The apparatus of claim 10, further comprising:

a conversion circuit to convert a first encoded condition into an approximated second encoding.

12. (Original) The apparatus of claim 10, further comprising:

a receiving circuit to receive an incoming signal, the receiving circuit to receive a third encoded condition and compensate the termination of the signal for the condition.

13. (Original) A system comprising:

a processor;

a first bus coupled to the processor;

a memory device;

a second bus coupled to the memory device; and

a memory controller coupled to the first and second buses, the memory controller having a programmable on die termination circuit.

14. (Original) The system of claim 13, wherein the memory controller can receive data over the second bus at a rate between 200 and 400 megatranfers per second (MTS).

15. (Original) The system of claim 13, wherein the memory controller further comprises a testing circuit to determine a condition in the memory controller and generate an encoded signal representing the condition, and

wherein the encoded signal set the programmable on die termination circuit.

16. (Original) A method comprising:

detecting a condition in a device;

generating an encoded signal representing the condition; and

programming an on die termination circuit to compensate for the condition.

17. (Original) The method of claim 16, further comprising:

converting the encoded signal into a driver signal to program the on die termination circuit.

18. (Original) The method of claim 16, further comprising:

receiving an external signal at a rate of 200 to 400 mega transfers per second (MTS) at the on die termination circuit; and

terminating the external signal.

19. (Original) A device comprising:

means for detecting a condition in a device;

means for generating an encoded signal based on the condition; and

means for programming an on die termination circuit based on the encoded signal.

20. (Original) The device of claim 19, further comprising:

means for converting the encoded signal into a driving signal to program the on die termination circuit.

21. (Original) The device of claim 19, further comprising:

means for receiving an external signal at a rate of 200 to 400 mega transfers per second (MTS) at the on die termination circuit; and

means for terminating the external signal.

22. (Original) A machine readable medium having instructions stored therein which when executed cause a machine to perform a set of operations comprising:

detecting a condition in a device;

generating an encoded signal representing the condition; and

programming an on die termination circuit to compensate for the condition.

23. (Original) The machine readable medium of claim 22, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

converting the encoded signal into a driver signal to program the on die termination circuit.

24. (Original) The machine readable medium of claim 22, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

receiving an external signal at a rate of 200 to 400 mega transfers per second (MTS) at the on die termination circuit; and

terminating the external signal.